COMMENTS

The enclosed is responsive to the Examiner's Final Office Action mailed on March 12, 2004. Applicant has: 1) added no claims; 2) amended claims 1, 2, 8, 9, 14 and 15; and 3) cancelled no claims. Claims 1-22 are pending.

35 U.S.C. §112 Rejections

Claims 1- 7 and 14-22 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Specifically, the Examiner has stated that element 1 of claim 1 and element 3 of claim 14 are not sufficiently described in the specification. The Applicant respectfully disagrees.

Page 11, lines 1-6 of the specification states...

> "Addresses for each of the data elements are then computed at 520 (**Figure 5**) by adding each of the indices to the base address stored in R2. Thus, in the embodiment illustrated in **Figure 7**, the base address is added to each of the indices in R5, R8, R11, and R14 and the result (i.e., the addresses in memory of each of the data elements) are stored in registers R6, R9, R12 and R15, respectively."

This shows that addresses are in fact computed by adding each indices to the base address. This would clearly qualify as a computation, which provides sufficient details to comply with the 35 U.S.C. §112, paragraph 1.

Further, page 12, lines 5-10 also show that address are in fact computed before being stored.

> "Referring to **Figure 10**, in one embodiment of the scatter operation, indices are extracted (at 1010) and added to a base address to compute the addresses in memory to which the data elements will be scattered (at 1020). This portion of the scatter operation may be similar to the first portion of the gather operation described above (e.g., 510, 520 of **Figure 5**)."

Through the above-cited language, the specification does in fact meet the written description requirements of 35 U.S.C. §112, paragraph 1 in regards to independent claims 1 and 14 and their dependent claims.

Claims 1- 7 and 14-22 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner state that claims 1 and 14 somehow compute addresses by storing data and that computing of data normally involves a computation and not just transferring of data. The Applicant respectfully disagrees. The same argument used for the 35 U.S.C. §112, paragraph 1 rejection applies here. Page 11, lines 1-6 and page 12, line 5-10 of the specification clarify what computation is

performed. The computation states that indices are added to a base address. This shows that an actual computation is occurring, and not just the transferring of data as stated by the Examiner.

Through the above-cited language, the specification does in fact meet the requirements of 35 U.S.C. §112, paragraph 2 in regards to independent claims 1 and 14 and their dependent claims.

35 U.S.C. §102 Rejections

Claims 1-4, 8-11, 14-17 and 21-23 stand rejected under 35 U.S.C. §102(b) as being anticipated by Austin, et al., U.S. Patent 3,163,850 (hereinafter, "Austin").

Austin describes a data processor that is capable of processing a gather instruction and a scatter instruction. The format used for the gather instruction, referred to as a Record Scatter variable ("RSV") instruction, is set forth at column 2, line 67 ("RSV Instruction RSV 0079 3011"). The data processor described in Austin includes dedicated address calculation hardware for processing the RSV instruction (emphasis added). For example, as described at column 5, lines 49-69, when an RSV instruction is encountered during the course of a program routine . . .

> It is fed along Information bus 15 into Program register 24 in the same manner as preceding instruction words. Immediately, the Op portion positions sign, 0 and 1, are interpreted by Operation Matrix 33 to initiate the RSV operation.

A musical chairs situation arises as address information is rearranged for the execution of the RSV instruction.
The result of the rearrangement is this:
The single block address is in Address register 29.
The address of the second RDW is in the Address Control register 92.
The first RDW is in the Record Definition register 51.
The RSV execution follows:
Read out data word from address specified by Address register 29 to the Arithmetic register 104. One-up Address register 29. Store data word (Arithmetic register) in working address per Start register 52. Increase working address by variable increment (Variable Increment register 101) and compare with Stop address (Stop register 53).

Thus, Austin describes a processor for processing gather and scatter instructions in an analogous manner to the CRAY-1 vector processor described in the background section of the present application, i.e., using dedicated address calculation registers to hold index vectors and dedicated address calculation hardware.

As stated in the previous amendment dated 01/12/04, Claim 1 recites a method for performing a gather operation which may be implemented on a general purpose processor and which does not require dedicated hardware. In Claim 1, the gather operation is performed via a plurality of individual instructions. More specifically, to "gather" the data elements stored in memory, an address calculation is performed in which each of a first set of instructions transfers a plurality of indices from a first storage location (e.g., a first general purpose register) where the indices are stored substantially contiguously, to an equal plurality of general purpose registers, wherein each index is assigned its own separate storage location. Then, each of a second set of instructions deposits one or more of the data elements contiguously with

other data elements within a general-purpose register. Similarly, Claim 14 claims a general-purpose computer system capable of performing a gather operation using a plurality of instructions rather than dedicated address generation hardware.

In addition, in contrast to Austin, Claim 8 recites a method for performing a scatter operation using a plurality of instructions. Specifically, Claim 8 recites

> . . . calculating addresses in memory to which a plurality of data elements are to be scattered to form a matrix in memory, wherein each address in memory is identified by one of a plurality of indices and a base address;
>
> executing a plurality of extract instructions, each of said extract instructions extracting one or more of said data elements from a storage location in which said data elements are stored contiguously to an equal plurality of separate storage locations; and
>
> transferring said data elements from said separate storage locations to said calculated addresses in memory.

In sum, Austin does not disclose any mechanism for performing a gather or scatter operation as recited in Claims 1, 8 and 14. Rather, Austin describes using dedicated address calculation registers and address calculation hardware to execute each gather and scatter operation.

Further, Examiner's *Response to Arguments* states, "Applicant claims that a plurality of instructions is used, but these instructions inherently utilize hardware – albeit not necessarily dedicated hardware. " Page 10, paragraph 29 of the office action dated 03/12/04. By this statement, Examiner has submitted that claims 1, 8 and 14 do not require the use of dedicated hardware. That is

what Applicant's are trying confirm. That Claims 1, 8 and 14 differ from Austin because of the distinction between the use of general purpose hardware versus dedicated hardware.

Accordingly, Applicants respectfully submit that Claims 1, 8 and 14 and all claims that depend from Claims 1, 8 and 14 are in condition for allowance.

CONCLUSION

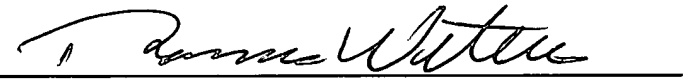
For the reasons provided above, Applicant respectfully submits that the current set of claims are allowable. If the Examiner believes an additional telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Thomas C. Webster at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 6/14/04



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